What is claimed is:

1. A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a capacitor electrically connected to the plug, the capacitor having a bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode; and

a reaction buffer layer between the first interlayer dielectric and the capacitor-ferroelectric layer.

2. The ferroelectric memory device of Claim 1, wherein the reaction buffer layer is adjacent to the side surfaces of the bottom electrode, and wherein a top surface of the reaction buffer layer and the top surface of the bottom electrode form a planar surface.

3. The ferroelectric memory device of Claim 2, further comprising a third interlayer dielectric under the reaction buffer layer, and wherein the reaction buffer layer comprises a material that prevents a reaction between the third interlayer dielectric and the capacitor-ferroelectric layer.

4. The ferroelectric memory device of Claim 2, wherein the reaction buffer layer is formed of a material selected from the group consisting of titanium oxide, tantalum oxide and aluminum oxide.

5. The ferroelectric memory device of Claim 2, further comprising:

a bit line that is electrically connected to the transistor on the first interlayer dielectric; and

a third interlayer dielectric recessed between the bottom electrode and a second bottom electrode associated with a capacitor of an adjacent ferroelectric memory device.

6. The ferroelectric memory device of Claim 5, wherein the reaction buffer layer is on the third interlayer dielectric.

7. The ferroelectric memory device of Claim 5, further comprising a

second interlayer dielectric between the first interlayer dielectric and the third interlayer dielectric, wherein the plug further penetrates the second interlayer dielectric to electrically connect the bottom electrode to the semiconductor substrate.

8. The ferroelectric memory device of Claim 1, further comprising a first diffusion barrier on the first interlayer dielectric and side surfaces of the bottom electrode.

9. The ferroelectric memory device of Claim 8, wherein the first diffusion barrier comprises an oxygen diffusion barrier.

10. The ferroelectric memory device of Claim 1, wherein the bottom electrode comprises:

a first material that serves as an oxygen diffusion barrier;

a second material for providing the capacitor-ferroelectric layer with oxygen on the first material; and

a third material having a lattice point that allows for formation of a capacitor-ferroelectric layer having a crystalline structure.

11. The ferroelectric memory device of Claim 10, wherein the first material is iridium, the second material is iridium oxide, and the third material is platinum.

12. The ferroelectric memory device of Claim 1, wherein the top electrode comprises a fourth material for providing the capacitor-ferroelectric layer with oxygen and a fifth material that is selected to improve the strength of the fourth material.

13. The ferroelectric memory device of Claim 12, wherein the fourth material is on the capacitor-ferroelectric and the fifth material is on the fourth material.

14. The ferroelectric memory device of Claim 12, wherein the fourth material is iridium oxide, and the fifth material is iridium.

15. The ferroelectric memory device of Claim 12, further comprising a second diffusion barrier on the capacitor-ferroelectric layer and on the top electrode.

16. The ferroelectric memory device of Claim 15, wherein the second diffusion barrier acts as a hydrogen diffusion barrier.

17. The ferroelectric memory device of Claim 16, wherein the second diffusion barrier comprises an aluminum oxide layer.

18. The ferroelectric memory device of Claim 1, further comprising:

a fourth interlayer dielectric on the top electrode;

a first metal line on a part of the fourth interlayer dielectric;

a fifth interlayer dielectric on the fourth interlayer dielectric;

a via hole that exposes the top surface of the top electrode; and

a second metal line in the via hole that is electrically connected to the top electrode.

19. The ferroelectric memory device of Claim 18, wherein the first metal line and the second metal line each comprise an aluminum metal line.

20. The ferroelectric memory device of Claim 5, further comprising a first contact pad between the bit line and the semiconductor substrate.

21. The ferroelectric memory device of Claim 20, wherein the first contact pad comprises a polysilicon contact pad.

22. The ferroelectric device of Claim 21, further comprising a second contact pad between the plug and the semiconductor substrate.

23. A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate that surrounds a gate electrode of the transistor;

a capacitor on the first interlayer dielectric, the capacitor comprising:

a buried bottom electrode on the first interlayer dielectric, the bottom electrode having a top surface and a plurality of side surfaces;

a capacitor-ferroelectric layer on the buried bottom electrode; and

a top electrode on the capacitor-ferroelectric layer;

a planarizing layer adjacent to the side surfaces of the bottom electrode, wherein a top surface of the planarizing layer and the top surface of the bottom

electrode form a planar surface and wherein the capacitor-ferroelectric layer is on the planar surface; and

a plug that penetrates the first interlayer dielectric under the bottom electrode, wherein the plug is electrically connected to the bottom electrode.

24. The ferroelectric memory device of Claim 23, wherein the planarizing layer comprises a reaction buffer layer.

25. The ferroelectric memory device of Claim 24, further comprising a third interlayer dielectric on the first interlayer dielectric and under the reaction buffer layer, wherein the reaction buffer layer comprises a material that prevents a reaction between the third interlayer dielectric and the capacitor-ferroelectric layer.

26. The ferroelectric memory device of Claim 25, wherein the reaction buffer layer is formed of a material selected from the group consisting of titanium oxide, tantalum oxide and aluminum oxide.

27. The ferroelectric memory device of Claim 24, wherein the bottom electrode comprises:

a first material that serves as an oxygen diffusion barrier;

a second material for providing the capacitor-ferroelectric layer with oxygen on the first material; and

a third material having a lattice point that allows for formation of a capacitor-ferroelectric layer having a crystalline structure.

28. The ferroelectric memory device of Claim 27, wherein the first material is iridium, the second material is iridium oxide, and the third material is platinum.

29. The ferroelectric memory device of Claim 24, wherein the top electrode comprises a fourth material for providing the capacitor-ferroelectric layer with oxygen and a fifth material that is selected to improve the strength of the fourth material.

30. The ferroelectric memory device of Claim 29, wherein the fourth material is iridium oxide, and the fifth material is iridium.

31. A method of fabricating a ferroelectric memory device, the method comprising:

forming a transistor on a semiconductor substrate;

forming a first interlayer dielectric on the semiconductor substrate and on the transistor;

forming a buried plug that penetrates the first interlayer dielectric;

forming a bottom electrode of a capacitor on the buried plug and the first interlayer dielectric;

forming a third interlayer dielectric on the first interlayer dielectric;

removing a top part of the third interlayer dielectric;

forming a reaction buffer layer on the third interlayer dielectric so that the side surfaces of the bottom electrode of the capacitor are covered by the reaction buffer layer;

forming a capacitor-ferroelectric layer on the reaction buffer layer and the bottom electrode; and

forming a top electrode of the capacitor on the capacitor-ferroelectric layer.

32. The method of Claim 31, wherein the top surface of the reaction buffer layer and the top surface of the bottom electrode are the same height above the semiconductor substrate.

33. The method of Claim 31, further comprising:

forming a bit line on a part of the first interlayer dielectric, the bit line being electrically connected to the substrate; and

forming a second interlayer dielectric on the first interlayer dielectric before formation of the third interlayer dielectric.

34. The method of Claim 33, further comprising forming a first diffusion barrier on the second interlayer dielectric and on at least the side surfaces of the bottom electrode after forming the bottom electrode.

35. The method of Claim 34, wherein the first diffusion barrier comprises an oxygen diffusion barrier.

36. The method of Claim 35, wherein the first diffusion barrier comprises an aluminum oxide layer.

37. The method of Claim 31, wherein forming the bottom electrode comprises:

depositing a first material that serves as an oxygen diffusion barrier on the first interlayer dielectric, depositing a second material that serves as an oxygen source for the capacitor-ferroelectric layer on the first material, and depositing a third material that has a suitable lattice point for formation of the capacitor-ferroelectric layer on the second material; and

selectively removing the first, second and third materials to form the bottom electrode.

38. The method of Claim 37, wherein the first material comprises iridium, the second material comprises iridium oxide and the third material comprises platinum.

39. The method of Claim 33, wherein forming the third interlayer dielectric comprises:

depositing a dielectric material on the second interlayer dielectric so as to cover the bottom electrode of the capacitor; and

planarizing the dielectric material to expose the top surface of the bottom electrode.

40. The method of Claim 39, wherein removing the top part of the third interlayer dielectric comprises removing the top part of the third interlayer dielectric that is adjacent to the bottom electrode using an oxide etch-back process so that the top surface of the third interlayer dielectric is lower than the top surface of the bottom electrode.

41. The method of Claim 31, wherein forming the reaction buffer layer comprises:

depositing a pre-selected material on the third interlayer dielectric and the bottom electrode; and

planarizing the top surface of the pre-selected material to expose the upper surface of the bottom electrode.

42. The method of Claim 41, wherein the pre-selected material is a

material that shields the capacitor-ferroelectric layer from reacting with the third interlayer dielectric.

43. The method of Claim 42, wherein the pre-selected material is at least one selected from the group consisting of titanium oxide, tantalum oxide and aluminum oxide.

44. The method of Claim 31, wherein forming the top electrode comprises:

depositing a fourth material on the capacitor-ferroelectric layer that provides the capacitor-ferroelectric layer with oxygen;

depositing a fifth material on the fourth material that enhances the strength of the fourth material; and

selectively removing the fourth and fifth materials.

45. The method of Claim 44, wherein the fourth material comprises iridium oxide and the fifth material comprises iridium.

46. The method of Claim 31, further comprising forming a hydrogen diffusion barrier on the top electrode and the capacitor-ferroelectric layer after forming the top electrode.

47. The method of Claim 46, wherein the hydrogen diffusion barrier comprises an aluminum oxide layer.

48. The method of Claim 31, further comprising:

forming a fourth interlayer dielectric on the top electrode;

forming a first metal line on a part of the fourth interlayer dielectric;

forming a fifth interlayer dielectric on the fourth interlayer dielectric and the first metal line;

selectively removing the fourth and fifth interlayer dielectrics to form a via hole that exposes a top surface of the top electrode; and

forming a second metal line that is electrically connected to the top electrode in the via hole.